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William E. Alford
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP
7th Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/749,088	ADACHI, MITSUHIRO	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20 and 21* is/are allowed.

6)☒ Claim(s) *1-12, 15-19 and 22-41* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07142004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and IDS both dated 7/14/2004.

2. Claims 1-41 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Applicant's arguments with respect to claim 1-41 have been considered but are moot in view of the new ground(s) of rejection.

5. Claims 1-9 and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas et al., U.S. Patent 6,216,235 in view of Casal et al., U.S. Patent 5,822,596.

6. As to claim 1, Thomas taught a method comprising:

a. generating a measure of global functional activity in an integrated circuit (measuring the temperature of the microprocessor, temperature is a measure of functional activity) [col. 3 lines 45-51];

b. determining if a predetermined limit of global functional activity (temperature due to activity) in an integrated circuit has been met or exceeded (temperature has become dangerously high) [col. 3 lines 21-30];

c. and if so, then:

i. gradually reducing a high frequency (FMAX) of clocking of circuitry to zero (the minimum frequency may be zero) to stop the clocking of circuitry [col. 3 line 52 through col. 4 line 22 and figure 2];

Thomas teaches detecting the temperature as a global functional activity. Thomas then teaches that if the temperature is met or exceeded the frequency of operation of clocking circuitry is then gradually reduced (including if necessary to a zero frequency).

Thomas does not expressly disclose waiting a predetermined time after stopping the clocking of circuitry and starting the clocking circuitry at a low frequency.

Casal teaches waiting a predetermine time (sufficient stabilization time) after stopping (powering down) the clocking of circuitry (for logic ciruits) and starting the clocking circuitry at a low frequency [col. 1 line 56-61, col. 1 line 56 through col. 1 line 4 and col. 3 line 58 through col. 4 line 11]. Specifically, Casal teaches determining the appropriate time spent at each frequency. In particular, Casal must start from a low frequency when the system is powered down. The system Casal is similar to that of Thomas in that the frequency of the processor is controlled. Casal waits a predetermined time after stopping the clock and starts a low frequency to protect against power surges and adequately allow for the system to dissipate heat generated during start up.

It would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Thomas and Casal before him, to modify Thomas by waiting a predetermined time after stopping the clock and starting the clocking circuitry at a low frequency as taught by Casal. Thomas and Casal are both directed toward controlling clocks of a computer

system. An artisan would have been motivated because Casal teaches that waiting for predetermined times between changing clock frequency and starting clocking circuitry at a low frequency avoids transients that are harmful in electronic components [col. 1 lines 16-21 and col. 1 lines 56-61]. Avoiding transients is desirable in computer systems such as Thomas.

7. As to claim 2, Thomas together with Casal taught the method according to claim 1 described above. Thomas further taught wherein if the determining if the predetermined limit of global functional activity in the integrated circuit has not been met or exceeded, it is repeated [col. 3 lines 38-lines 67]. Thomas discloses using a temperature sensor to determine if the limit has been met or exceeded. In doing so, Thomas clearly must continually determine the temperature. In Thomas, the determining step must be repeated to determine a change in temperature. This would be especially true if the limit has not been met or exceeded.

8. As to claim 3, Thomas together with Kenny and Inoue taught the method according to claim 1 described above. Thomas and Casal do not expressly disclose wherein the predetermined time is a number of clock cycles of a free-running clock of the integrated circuit. However, both Thomas and Casal each use a free-running clock. Casal teaches at col. 4 lines 1-11 that an appropriate amount of time is required at each frequency of operation. One of ordinary skill in the art would have recognized that a free-running clock is used to measure time by counting its clock cycles. It would have been obvious to one of ordinary skill at the time of the invention to use the free-running clock to determine the predetermined time using a number of clock cycles of the free running clock of the integrated circuit because the free-running clock is an available mean to determine time and is readily available in the existing circuitry.

9. As to claim 4, Thomas together with Casal taught the method according to claim 1 described above. Thomas further taught at col. 12, lines 3-7, and Casal taught at col. 1, lines 56-61, the gradual reducing of the high frequency clocking of circuitry to zero includes:

a. clocking the circuitry at a first frequency; and

b. before clocking the circuitry at a second frequency lower than the first frequency, waiting a predetermined time during the clocking of the circuitry at the first frequency.

Specifically, Thomas discloses "... a controllable frequency of the clock is gradually and *successively stepwise reduced* as needed to regulate thermal conditions." Successively stepwise reduced clearly implies, or at the very least an artisan would recognize that it implies, that in reducing the clock frequency the clock is reduced to lower frequencies only after waiting a predetermined time at a particular frequency.

Casal discloses that a clear need, which his invention satisfies, is a "... system and method for accomplishing a *step-by-step increase and* ***decrease*** *of a clock frequency*... such that a *sufficient number of steps and sufficient stabilization time* at each step is provided..." Step-by-step increase and decrease with sufficient stabilization time clearly teaches changing frequencies from a first frequency to a lower second frequency only after waiting a predetermined time.

10. As to claim 5, Thomas together with Casal taught the method according to claim 1, described above. Casal further taught at col. 1, lines 56-61, wherein after starting the clocking of the circuitry at the low frequency, the method further includes gradually increasing the frequency of the clocking of the circuitry to the high frequency. Specifically, Casal taught that the step-by-step change in the clock frequency would also be applied during a startup of the system.

11. As to claim 6, Thomas together with Casal taught the method according to claim 5 described above. As set forth hereinabove for the same reasons, Casal also teaches the gradual increasing of the frequency of circuitry to the high frequency includes clocking circuitry at a first frequency, and before clocking the circuitry at a second frequency higher than the first frequency, waiting a predetermined time during clocking of the circuitry at the first frequency. Specifically, Casal teaches that the step-by-step increase would be applied at startup.

12. As to claim 7, Thomas together with Casal taught the method according to claim 1 described above. Thomas further taught at col. 7, lines 13-34, wherein the global functional activity (temperature due to activity) in the integrated circuit is proportional to temperature of the integrated circuit (microprocessor) and the predetermined limit (temperature is determined to be "hot") of global functional activity is proportional to an expected temperature of the integrated circuit. Thomas discloses using a temperature sensor that is integrated with a microprocessor circuit. The sensor is used to determine the temperature due to processing activity.

13. As to claim 8, Thomas together with Casal taught the method according to claim 1, described above. Thomas inherently teaches wherein the gradual reducing of the high frequency clocking of the circuitry to zero avoids large variations in the current associated with a rapid shut-off of the clocking of circuitry. Thomas gradually reduces the clock frequency that must avoid large variations in the current as those associated with a rapid shut-off of the clocking circuitry. Casal also teaches at col. 1, lines16-21 and col. 1, line 56 through col. 1, line 4, gradually decreasing a high frequency to zero using a step-by-step decrease thereby avoiding current transients during a shutdown.

14. As to claim 9, Thomas together with Casal taught the method according to claim 5 described above. Casal further taught at col. 1, lines16-21 and col. 1, line 56 through col. 1, line 4 the starting (when powering up) of the clocking of the circuitry at the low frequency and the gradual increase in the frequency of the clocking of the circuitry to the high frequency avoids large variations in current (current surge) otherwise associated with a rapid turn-on of the clocking of circuitry.

15. As to claims 22-26, applicants have submitted on page 29 of the remarks that the claims are well known and are supported. Therefore, they are rejected because they are well known in the prior art.

16. Claims 10-12, 15-17 and claims 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas in view of Mittal et al., U.S. Patent 5,719,800 (cited in IDS dated 7/14/2004).

17. As to claim 10, Thomas teaches a circuit comprising:

a. a clock generator (oscillator 8, 22, 52 and clock input of different embodiments) to generate a clock [figures 1, 3, 4, 5, 9 and 10];

b. an activity detector to measure global functional activity of the circuit and temperature sensor (temperature due to processor activity) [figures 3, 5, 7, 9, and 10; col. 4 lines 30 et seq.];

c. a clock throttling controller (inherently within oscillator 8 to produce a clock signal that will gradually reduce) [col. 4 lines 1-22, col. 7 line 42-44, figures 1-3 and 9] coupled to the activity detector and the clock generator, the clock throttling controller to generate

a throttled clock to couple to the circuit for clocking circuitry therein, the clock throttling controller to gradually throttle the frequency of the throttled clock to the circuit in response to the measure of the global functional activity meeting or exceeding (temperature is too high) a predetermined limit [col. 4 lines 8-10].

Thomas teaches wherein the temperature (caused by high activity) causes the clock to be gradually throttled in response to activity. If the activity were very high for a sustained period of time the temperature would reach above a predetermined threshold causing throttling to take place [col. 4 lines 1-22].

It is interpreted that Thomas would have functional blocks within the microprocessor. As is well known in the art and as would be appreciated to those of ordinary skill in the art a microprocessor includes many functional blocks such a I/O devices for receiving and outputting data, arithmetic units and instruction decoder. A microprocessor contains at the very minimum a CPU and I/O devices for inputting and outputting data. The CPU further contains at the very minimum an instruction decoder (to receive and decode the instruction), an input/output device to move data and instructions to and from memory, and an arithmetic logic unit to perform processing. However, Thomas does not expressly disclose multiple functional blocks.

Mittal teaches a VLSI microprocessor that contains multiple functional blocks [col. 2 lines 14-19 and col. 3 lines 4-8]. Mittal further teaches that if it is desired to monitor the overall power consumption of an IC, then it substrate temperature would be measured and this value would be used as the activity level [col. 5 lines 39-43]. The system of Mittal is similar to that of Thomas in that both systems use a VLSI microprocessor. Mittal if further similar to Thomas in

that if it is desired to monitor the overall power consumption of an IC, then it substrate temperature would be measured and this value would be used as the activity level [col. 5 lines 39-43]. Mittal provides the advantage of dynamic power/speed tradeoff across multiple functional units to avoid reliability problems, heat dissipation and power supply problems.

It would have been obvious to one of ordinary skill in the art, having the teachings of Thomas and Mittal before them at the time the invention was made, to modify Thomas by substituting his microprocessor circuit with the microprocessor circuit as taught by Mittal. One of ordinary skill in the art would have been motivated to make this modification in to take advantage of the dynamic power/speed tradeoff across multiple functional units to avoid reliability problems, heat dissipation and power supply problems. in view of the teaching of Mittal.

Thomas does not expressly disclose wherein the clock generator, activity detector and clock throttling controller are on an integrated circuit. Official Notice is taken of the motivation and modification necessary to integrate devices on an integrated circuit, this is notoriously well known. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Thomas by manufacturing the clock generator, the activity detector and the clock throttling circuit on the same integrated circuit because integrated circuits often have a plurality of different devices. One of ordinary skill in the art would have made the modification because one of ordinary skill would have recognized that doing so would reduce cost, increase speed and increase reliability all of which would be highly desirable in Thomas.

18. As to claim 11, Thomas together with Mittal as set forth hereinabove, taught the integrated circuit as according to claim 10. Mittal teaches using temperature as a measure of the

activity of a plurality of functional blocks. Thus, Mittal teaches that activity detector receives measures of local functional activity (heat generated by each of the functional blocks) associated with each functional block of the integrated circuit to measure the global functional activity [col. 5 lines 38-43].

19. As to claim 12, Thomas together with Mittal as set forth hereinabove taught the integrated circuit according to claim 10. Mittal teaches using temperature as a measure of the activity of a plurality of functional blocks [col. 5 lines 39-43]. Specifically, the activity detector (sensing temperature) receives measures of local activity associated with each functional block (heat produced by each functional block contributes to the temperature) of the integrated circuit to determine the measure of the global functional activity of the integrated circuit (the temperature is used as the activity level).

20. As to claim 15, Thomas together with Mittal taught the integrated circuit according claim 10, described above. Thomas teaches wherein one hundred percent of circuitry in the processor can have the throttled clock stopped. Specifically, Thomas teaches that the clock to the microprocessor may be stopped. Thomas discloses that the clocks can be set to a sleep clock that near the minimum frequency fMIN [col. 4 lines 1-14]. Thomas also discloses wherein fMIN may be zero [col. 4 lines 5-7]. Thus, when combined with Mittal one hundred percent of the circuitry in the functional blocks would be stopped.

21. As to claim 16, Thomas together with Mittal taught the circuit according to claim 10 described above. Thomas teaches gradually throttling clocks of a integrated circuit within his processor. Mittal further taught wherein less than one hundred percent of the circuitry in the functional blocks can have the throttled clock stopped [col. 10 lines 28-42]. Specifically, Mittal

teaches that functional blocks such as speculative instruction cache prefetching may be disabled if the activity level monitor is exceeded. Both Thomas and Mittal use temperature as an activity level monitor.

As to claim 17, Thomas together with Mittal taught the circuit according to claim 16, described above. Mittal teaches an integrated circuit with functional blocks. As combined with Thomas if the temperature of the IC due to the heat of the functional blocks is above a predetermined limit one hundred percent of the clocks would be stopped as taught by Thomas.

22. As to claim 27, Thomas and/or Thomas together with Mittal taught the integrated circuit according to claim 10. Thomas further teaches that the limit is proportional to a well known temperature level for integrated circuits [col. 4 line 10].

23. As to claims 28-32, applicants have submitted on page 29 of the remarks that the claims are well known and are supported. Therefore, they are rejected because they are well known in the prior art.

24. As to claim 33, Thomas together with Mittal taught the integrated circuit according to claim 10. Thomas teaches the clock throttling controller gradually throttles down the frequency of the throttled clock to zero (the minimum frequency may be zero) in response to the measure of the global functional activity meeting or exceeding the predetermined limit [col. 4 lines 1-10].

25. Claim 18 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas in view of Mittal and Casal.

26. As to claim 18, Thomas and/or Thomas together with Mittal taught the integrated circuit according to claim 10 described above. Thomas further taught wherein, the frequency of the

throttled clock is gradually throttled OFF in response to the measure of the functional activity (temperature is a measure of functional activity) meeting or exceeding the predetermined limit [col. 4 lines 8-14]. In summary, Thomas gradually throttles up a clock when activity is below a certain predetermined level. Thomas gradually throttles down a clock when activity is above a certain predetermined level. However, Thomas describes that the system clock is responsive to the activity (the temperature of the integrated circuit) meeting or exceeding the predetermined limit (the speed of the clock in Thomas is responsive to the measures temperature). Thomas further describes that the clock (VCO 8) is temperature-regulated and responds in an intelligent manner to prevent overheating [col. 4 lines 46-64]. Therefore it is throttled in response to the temperature of the integrated circuit.

Thomas does not expressly disclose and after being off for a predetermined period of time, the throttled clock is then gradually throttled ON.

Casal teaches after being of for a predetermine time (sufficient stabilization time) after stopping (powering down) a throttled clock is then gradually throttle ON [col. 1 line 56-61, col. 1 line 56 through col. 2 line 4 and col. 3 line 58 through col. 4 line 11]. Specifically, Casal teaches determining the appropriate time spent at each frequency. The system Casal is similar to that of Thomas in that the frequency of the processor is controlled. Casal waits a predetermined time after stopping the clock and gradually throttles up the clock frequency to protect against power surges and adequately allow for the system to dissipate heat generated during start up. Further, the teachings of Casal would provide the hysteresis suggested by Thomas for gradually throttling the clocks back ON.

It would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Thomas and Casal before him, to modify Thomas by waiting a predetermined time after gradually throttling OFF the clocks, then gradually throttling the clocks ON taught by Casal. Thomas and Casal are both directed toward controlling clocks of a computer system. An artisan would have been motivated because Casal teaches that waiting for predetermined times between changing clock frequency and starting clocking circuitry at a low frequency avoids transients that are harmful in electronic components [col. 1 lines 16-21 and col. 1 lines 56-61]. Avoiding transients is desirable in computer systems such as Thomas.

As set forth, Thomas teaches throttled clock is gradually throttled off. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Thomas by throttling the clock to zero frequency to further reduce power consumption as desired by Thomas. An artisan would recognize that having a environment where the clocks are reduce to zero that the clock must also be throttled on when activity reaches the predetermined level resulting in the claimed invention.

27. As to claim 34, Thomas together with Mittal and Casal taught the integrated circuit according to claim 10. Thomas together with Mittal does not expressly disclose wherein after a predetermined time with frequency of the throttled clock at zero, the clock throttling controller gradually throttles up the frequency of the throttled clock from zero.

Casal teaches after being of for a predetermine time (sufficient stabilization time) after stopping (powering down) a throttled clock is then gradually throttle ON [col. 1 line 56-61, col. 1 line 56 through col. 2 line 4 and col. 3 line 58 through col. 4 line 11]. Specifically, Casal teaches determining the appropriate time spent at each frequency. The system Casal is similar to that of

Thomas in that the frequency of the processor is controlled. Casal waits a predetermined time after stopping the clock and gradually throttles up the clock frequency to protect against power surges and adequately allow for the system to dissipate heat generated during start up. Further, the teachings of Casal would provide the hysteresis suggested by Thomas for gradually throttling the clocks back ON.

For the same reasons as set forth above it would have been obvious to modify Thomas and Mittal with Casal.

28. Claims 19 and 37-41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas in view of Bailey U.S. Patent 5,451,892.

29. As to claim 19, Thomas teaches:

a. an activity detector (thermal sensor) to receive measures of local functional activity (temperature is a measure of functional activity in Thomas) associated with an integrated circuit and generate a total measure of functional activity of the integrated circuit, the activity detector to determine whether or not the total measure of functional activity exceeds a predetermined limit of activity (temperature threshold) to enable a throttling signal (above a predetermined temperature threshold) [figures 2, 3 and 9, and col. 4 lines 8-14]; and

b. a clock throttling controller coupled to the activity detector and the clock throttling control to generate a throttled clock to couple to the functional blocks of the integrate circuit for clocking circuitry therein, the clock throttling controller to gradually throttle

the frequency [col. 4 lines 9-11] of the throttled clock to circuitry of the in response to the enable throttling signal.

Thomas does not expressly show free-running clock generator to generate a free-running clock or that the free-running clock generator is coupled to the activity detector and a clock throttling controller. Specifically, Thomas discloses using a VCO rather than a free-running clock. Thomas also does not expressly disclose using functional blocks as set forth above.

Bailey teaches a clock generator comprising a free-running clock to generate a free-running clock generator (external clock) to generate a free-running clock and that the free-running clock is coupled to an activity detector (thermal sensor 134 – detecting the overall activity of the integrated circuit) and clock throttling controller (clock management unit along with PLL 122 and circuit divider). Bailey teaches a system similar to that of Thomas. Both are directed to reducing the clock frequency to an integrated circuit. Bailey suggests to those of ordinary skill in the art that other types of clock sources may be used to control the frequency of an integrated circuit. Those of ordinary skill in the art will appreciate that the clock of Bailey would suggest that his free-running clock would be used to other portions of the computer system that do not need or require clock throttling while throttling is occurring. Thus using the teachings of Bailey an advantage of using only one clock is gained. Bailey further teaches that the activity detector and clock throttling controller may be integrated together. Advantages of integrating circuitry, as appreciated by those of ordinary skill, include reducing power consumption, using less die space, increasing speed of processing signals and reducing cost.

Bailey teaches a CPU core with functional blocks [col. 4 lines 41-46]. Bailey teaches using a 80486 as the CPU core, which has a plurality functional blocks.

It would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Thomas and Bailey before them, to modify Thomas by using the clock generator comprising free-running clock of Bailey to achieve the advantage of requiring only one clock generator for the computer system and other advantages such as reducing power consumption, using less die space, increasing speed of processing signals and reducing cost.

30. As to claim 35, Thomas together with Bailey taught the integrated circuit according to claim 19. Thomas further teaches the clock throttling controller gradually throttles down the frequency of the throttled clock to zero (the minimum frequency may be zero) in response to the measure of the global functional activity meeting or exceeding the predetermined limit [col. 4 lines 1-10].

31. As to claims 37-41, applicants have submitted on page 29 of the remarks that the claims are well known and are supported. Therefore, they are rejected because they are well known in the prior art.

32. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas in view of Bailey and Casal.

33. As to claim 36, Thomas together with Bailey taught the method according to claim 35. Thomas together with Bailey does not expressly disclose wherein after a predetermined time with frequency of the throttled clock at zero, the clock throttling controller gradually throttles up the frequency of the throttled clock from zero.

Casal teaches after being of for a predetermine time (sufficient stabilization time) after stopping (powering down) a throttled clock is then gradually throttle ON [col. 1 line 56-61, col. 1 line 56 through col. 2 line 4 and col. 3 line 58 through col. 4 line 11]. Specifically, Casal teaches determining the appropriate time spent at each frequency. The system Casal is similar to that of Thomas in that the frequency of the processor is controlled. Casal waits a predetermined time after stopping the clock and gradually throttles up the clock frequency to protect against power surges and adequately allow for the system to dissipate heat generated during start up. Further, the teachings of Casal would provide the hysteresis suggested by Thomas for gradually throttling the clocks back ON.

For the same reasons as set forth above it would have been obvious to modify Thomas and Bailey with Casal.

Response to Arguments

34. Regarding claim 1, applicants argue in substance that Thomas does not disclose "generating a measure of global functional activity in an integrated circuit" and determining if a predetermined limit of global functional activity in the integrated circuit has been met or exceeded" as recited in amended claim 1. The examiner does not agree with applicants.

Thomas teaches the generating a ***measure*** of global functional activity in an integrated circuit by measuring the temperature. As is recognized by those of ordinary skill the temperature is a measure of global functional activity. Specifically, temperature is proportional to the activity of an integrated circuit.

Thomas determines if a predetermined limit of global functional activity (the temperature of the chip is above, for example 120 degrees F) has been met or exceeded [col. 3 lines 21-30 and col. 4 lines 8-14]. Applicant state that the temperature sensor is either within the housing or in contact with the housing or package thereof, which further shows that the temperature is a measure of the global functional activity.

Applicants further argue in substance that the temperature sensor of Thomas does not disclose receive activity levels from functional blocks within an integrated circuit. Even if Thomas does not teach receiving activity levels from functional blocks within an integrated circuit this argument is moot because it is noted that the features upon which applicant relies (i.e., "receiving activity levels from functional block") are not recited in claim 1 that has been rejected.

Applicants also argue in substance that Casal does not disclose that the waiting a predetermined time period after stopping clock the clocking of circuitry and starting the clocking of circuitry at a low frequency. The examiner does not agree. Casal teaches at col. 3 line 66 through col. 4 line 11. That heat levels are taken into consideration when determining when to start and stop clock signals and the amount of time required at each frequency. When combined with Thomas one of ordinary skill would realize that if the clock is stopped because the temperature was above a limit the system should not start for at least a predetermined time allowing the system to cool to an appropriate temperature.

35. As to claim 10, the common knowledge or well-known in the art statement concerning the limitation of integrating the clock generator, activity detector and clock throttling controller

on a single circuit is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice.

Further as to claim 10, the following arguments are with respect to the changes of the rejections. Thomas measures the temperature of a microprocessor due its activity. The activity is global because the microprocessor, as is known to those of ordinary skill, has many functional units within it. All of the functional units contribute to the temperature when they are active. Therefore the temperature sensor detects a measure of global functional activity.

Applicants further argue in substance that the temperature sensor of Thomas may be influenced from other sources such as high currents into large loads. The examiner agrees. However, if the high current is due to a large load it merely means that the activity being performed is large activity. The large activity causes a high temperature than a small activity and thus the temperature is a weighted measure of global functional activity. Thus, it is still a measure of the global activity of the integrated circuit.

Applicants argue that there is a time delay in the generation of the measure of any temperature signal in Thomas. The examiner does not disagree. However, this argument is moot because it is noted that the features upon which applicant relies (i.e., there no time delay in measuring activity) are not recited in claim 10 that has been rejected.

36. As to claim 18, it appears that applicants argue in substance that a free running clock would not have zero frequency. It is noted that the features upon which applicant relies (i.e., "free running clock") are not recited in claim 18 that has been rejected.

Allowable Subject Matter

37. Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

38. Claim 20-21 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703)308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
October 4, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600 2 KO